Design Trends of a Low Power Successive Approximation Register Analog-to-Digital Converter

Saima Bashir
Department of Electronics and Communication Engineering, National Institute of Technology, Srinagar, India

Suhaib Ahmed
Department of Electronics and Communication Engineering, Shri Mata Vaishno Devi University, Katra, India

Vipan Kakkar
Department of Electronics and Communication Engineering, Shri Mata Vaishno Devi University, Katra, India

Abstract – It is a well-known fact that Analog-to-Digital Converters (ADCs) consume around 30% of the total power of the analog front end of a device. Hence, reducing the power consumption is the key step towards Low and Ultra Low power applications. One typical ADC that has been gaining attention for its capability of low power operation is Successive Approximation Register (SAR) ADC. In this paper, a survey of the state-of-the-art experimental and the commercially available Successive Approximation Register (SAR) as a low power Analog to Digital Converter has been presented. This paper also discusses the various design techniques proposed till date to achieve this goal while keeping a close eye on their effect on the performance parameters of ADC. It is observed that there is a trade-off between power, area, resolution and sampling rate depending upon the design specifications and application required.

Index Terms – ADC, SAR, Low Power, Sampling Rate, Resolution, Figure of Merit, ENOB

1. INTRODUCTION

Analog to Digital converters are ubiquitous critical components of Signal Processing Systems as they convert the signals of real world to the digital domain. Be it the field of Telecommunication or Optical Networking, Data acquisition system or speech processing, audio processing or video processing, biomedical engineering or instrumentation, Data Converters are critical components of all such integrated systems and since the last three decades there has been a rapid advancement in the success of such systems. Based on the parameters which decide the performance of these Data Converters, there exists a variety of Analog to Digital Converters. One of the Analog to Digital Converters, SAR, famous for its operation at low power is discussed in this paper.

Successive Approximation Register (SAR) Analog to Digital Converter (ADC) is a counter type of Data Converter where the binary values are counted till the value of counter reaches the value approximately equal to the input Analog value. However this type of ADC differs from other Counter type ADC's as here instead of starting the count in sequence, the counter runs in such a way that the value of bits change one after the another, starting at Most Significant Bit (MSB) and ending at Least Significant Bit (LSB).

The architecture of SAR ADC, as shown in figure 1, consists of a Sample and Hold circuit, followed by a Comparator, a Successive Approximation Register that acts as a digital control logic and a Digital to Analog Converter (DAC) in feedback. The signal at the input is sampled using a Sample and Hold Circuit, thus converting the input signal from Analog to Discrete domain; Comparator compares the present sampled input value to the previous value in SAR logic register; Successive Approximation is a digital control unit used to generate the bits in sequential manner; and DAC converts the output back to Analog domain to provide the feedback.

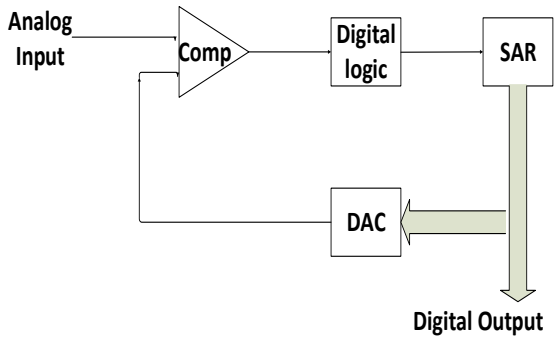

Figure 1 Architecture of SAR ADC

The working of SAR ADC is explained as under: The conversion of Analog Signal to its Digital counterpart starts with the Sampling of Input Analog signal. As the system receives the first sample, the digital control register generates the first word, with the MSB at logic high and all other bits at logic low. The DAC converts the word back to Analog form thug giving the voltage of 0.5Vref as the other input to comparator. The comparator compares this value to the input sample and depending on whether the sample value is greater

or less than the logic word the first bit of the output is set at logic level '1' or '0' respectively. This determines the value of MSB. Now using the current value of MSB, setting the 2nd bit at logic high and the rest of all bits at logic low, the next word is formulated. This word after being converted back to Analog form is compared to the sample again and the output decides the value of 2nd MSB. In this way comparison goes on and on until all the bits are decided and the final word in the register gives the approximate digital value of the Sample. Figure 2 explains how the Successive Approximation Register works.

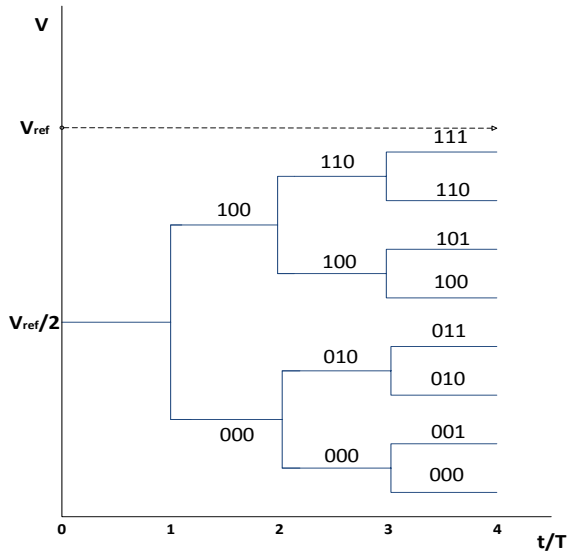

Figure 2 Working of SAR ADC

Unlike the other types of Counter ADC, where the conversion time is the function of Amplitude of Sampled input, here each sample takes N cycles to convert itself to a Digital Value, where N is the Resolution of Data Converter. Because of the complexity of the design, SAR ADC is an expensive Data Converter but due to its ability to consume the least power, it is the most widely used type of Data Converter.

2. PERFORMANCE PARAMETERS

All the related works that have been done by other researchers that are related to the current research problem should be summarized in this section. Sub topic 3

2.1. Resolution

The resolution of the Data converter indicates the number of discrete values it can produce over the range of Analog physical values. The resolution of the ADC is defined by the LSB voltage, which is the minimum change in voltage required to guarantee a change in the output code level. Generally the resolution of SAR lies between 8 and 12 bits, however certain design specifications can be used to increase the resolution up to 16 bits.

2.2. Sampling Rate

The rate at which new digital values are sampled from the Analog signal is called the sampling rate or sampling frequency of the Data converter. It is the maximum rate at which samples of the input data can be attained by the Data converter circuitry to operate and produce the correct output. According to the definition of Shannon-Nyquist sampling theorem, the faithful reproduction of the signal is possible only if the sampling rate is equal to or higher than twice the highest frequency of the signal.

2.3. Power Consumption

Power consumption is the rate at which electrical energy is utilized in a circuit. Power consumption increases proportionally with frequency. ADCs can consume a large percentage of power in a receiver, therefore it is of vital interest to minimize ADC power consumption. Current work done in this field has reduced the Power Consumption to the order of nano-watts.

2.4. Signal-to-Noise Ratio (SNR)

How accurately a Data Converter can measure a signal relative to the noise it introduces, gives the measure of its Signal to Noise Ratio SNR is measured in logarithmic (decibel) units

3. LOW POWER SAR DESIGN TECHNIQUES

The entire proposed modelling and architecture of the current research paper should be presented in this section. This section gives the original contribution of the authors. This section should be written in Times New Roman font with size 10. Accepted manuscripts should be written by following this template. Once the manuscript is accepted authors should transfer the copyright form to the journal editorial office. Authors should write their manuscripts without any mistakes especially spelling and grammar.

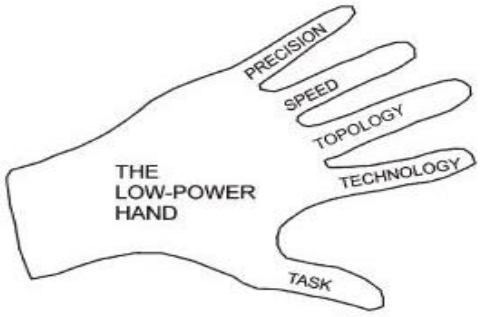

Figure 3 Low Power Hand [15]

In order to design any system at desired constraints, we need to gain the deep knowledge of the circuit. The constraints laid on the performance of the SAR ADC are given in terms of a LOW POWER HAND, as shown in figure 3, where five fingers of

hand represent five characterisations, i.e. Task or Application, Technology used, Architecture of Data Converter, Speed or Sampling rate and Accuracy or Precision.

In this paper we will discuss certain principles used by different scholars in order to make SAR ADC a Power- efficient design.

3.1. Principle of Charge Distribution in DAC

In a converter based on principle of charge distribution Binary weighted Resistors are replaced by Binary Weighted Capacitors, and several techniques are applied to reduce the power consumption, which include:(1) reducing the size of the capacitors, (2) precharging the capacitors, (3) recycling the charge stored in the capacitor, (4) performing the monotonic switching (set-and-down), (5) Merged capacitor switching method, and (6) the VCM-based switching method. One of the proposed architecture for 8-bit successive approximation Analog-to-Digital converter (ADC) in a standard 0.13 µm CMOS process technology at sample rates exceeding 60kS/s makes use of sub-threshold transistor operation to achieve ultra-low (Nanowatt range) power consumption[4].

The most effective way to reduce circuit power consumption and increase the speed is to minimize the capacitance of the internal DACs. One of the ways to reduce the effective unit capacitance value is to use a two-stage weighted capacitor network and C-2C capacitor network. The two-stage weighted capacitor network consists of capacitor banks each for coarse bits and fine bits, connected in series by a coupling capacitor [12]

The capacitor array also determines the accuracy of the data converter, which is based on the matching and noise in Capacitors. In some experiments, Poly–poly capacitors were used with the top plates acting as the common plate to minimize parasitic capacitance at the comparator input of Smart Dust Mote and energy consumption was decreased to Pico joule range, the lowest recorded at that time [11].

Reduction in delay and power is also achievable with the use of Low-k Dielectrics. The effect of dielectric absorption of a special material or its impact on the functionality of a circuit when studied in contrast to SAR ADC, it was found that high dielectric absorption leads to high resolution. Based on this concept, a 16-bit differential ADC was introduced, which allow fast and accurate conversions [14].

3.2. Switched Capacitance based Sample and Hold Design

Several energy-efficient switching methods have been proposed from time to time to lower the switching energy of the capacitor network, e.g. the split capacitor method, which reduces switching energy by 37%; the energy-saving method, which reduces energy consumption by 56% and monotonic switching method, which reduces power consumption by 81% without splitting or adding capacitors and switches [2]. Figure 4 shows the difference between normal architecture and one of the Switched Capacitance architecture. Using this technique, an SAR ADC has been proposed that consumes less than 0.34mW of Power at 1 V for a sampling rate of 50 kS/s [1].

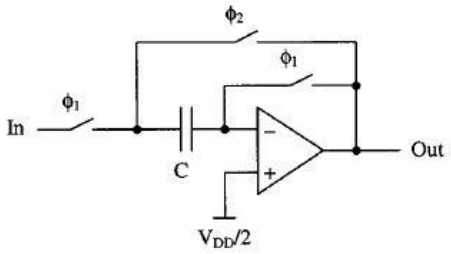

Figure 4 Conventional Sample and Hold Circuit [1].

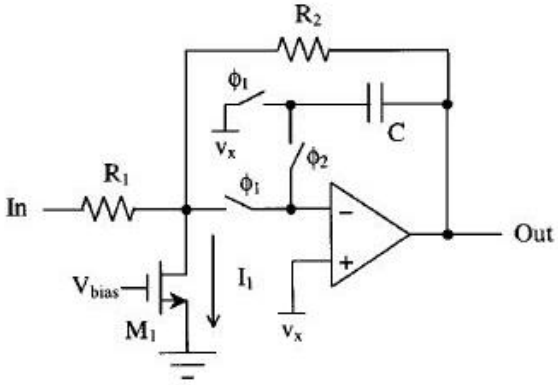

Figure 5 Low Power Sample and Hold Circuit [1].

In the research conducted for Low power Smart Dust, the switch network was built with simple nMOS devices for the ground reference, pMOS for the supply reference, and CMOS switches for the input signal and no gate boosting was used. It was found that the simulated energy consumption of switching network of SAR at 1 V and 100 kHz is 8.7pJ [11].

Similarly reduction in Power consumption is achieved in biomedical applications by replacing Monotonic switching speed by Capacitor-constructed Bypass-window scheme [13].

3.3. Optimal Supply Voltage

Lowering the supply voltage is an effective strategy for reducing the power consumption of circuits and the contribution of ADC strongly impacts the overall energy profile. Besides the reduction in power consumption, with the optimum supply voltage conductance of Analog transmission switches is drastically reduced and reliability is increased [9].

3.4. Dedicated MOS Structure

Applications using broadband digital wireless modulation require high-resolution low-power ADC over a bandwidth of few megahertz, hence CMOS in certain such application is replaced by High Performance Analog Thin-oxide MOS,

known as HPA TMOS. A low-power 1.2V ADC has been implemented in a 65nm CMOS process to achieve 10 bit resolution at 100MS/s based on the use of dedicated HPA MOS transistor [10].

3.5. Hybrid Architecture

In a Hybrid Architecture such as a fully differential SAR and Dual-Slope Hybrid ADC, the trade-offs among resolution and power consumption are relaxed. Dual-slope ADC is famous for its conversion at high resolution (>16 bits) whereas SAR boosts up the conversion speed at a very low power consumption. In one of the proposed architecture, a hybrid ADC is proposed for biomimetic microelectronic systems using 0.18um CMOS process, where SAR and Dual-Slope architectures are combined to achieve 12 bit resolution at 50kS/s Sampling rate and Power consumption of approximately 60µW [5].

3.6. Rail-to-Rail Comparator

Conventional comparators are implemented using differential input devices where n-type input or p-type input is chosen depending on the signal dc bias level, but both the n-type as well as p-type input comparator can handle only half polarity of signal range. In current research scenario, n-type and p-type are merged to handle rail-to-rail input range due to which it has become possible to solve the kickback noise and to reduce the power consumption by 52% to 80%. SAR ADC using Rail-to-Rail Comparator along with Adaptive Power Control technique, for biomedical application, has been implemented in 0.18µm TSMC CMOS technology which consumes 2.86 µW at 250kS/s and the figure of merit is 85.7 fJ/conversion-step [7].

3.7. Current Mode Operation

The circuit in which an input is a current I_{in}, obtained by using a current-mode Sample and Hold (S&H) element is known as Current Mode Architecture. In this work, the input current is compared in each SAR stage with a reference current I_{ref}, which is obtained as an output of the Current Mode DAC. The advantages of this principle is noise rejection and that, good matching between transistors is not critical, as any mismatch in these pairs can be easily compensated by adjusting current during device calibration. An ADC has been proposed that adjusts to operate with different sampling frequencies ranging from 100 kHz to 250 kHz, but at an frequency of 1.25 MHz, the circuit operates in optimum energy range at an 8-bit resolution with power dissipation ranging from 220nW to 550nW for a 0.55 V power supply[8].

3.8. Dual Supply Voltage

The power consumption in digital circuits can be about 20 percent to 80 percent of the total power consumption of SAR ADCs. Thus, Power can be decreased by designing the digital part of system, i.e. Successive Approximation control circuitry at the voltage different from the supply voltage used by the Analog components of the system. One such research was conducted in 2012 that shows by the use of dual-supply voltage, 1.0 V for Analog and 0.4 V for digital components, the ADC Power Consumption reduced to 53 nW at a sampling rate of 1 kS/s and it achieved the ENOB of 9.1 bits [3].

3.9. Tri-level Comparator

The tri-level comparator uses the meta-stable state to realize a fast, low power, and small area using only one comparator. Tri-level comparators are used in search algorithms that use three output levels of high, middle, and low. The metastable detector (MD) consists of XNOR, digitally tunable delay element, and D-Flip-Flop. The Tri-Level comparator along with reconfigurable DAC architecture has greatly reduced the power consumption of the ADC and enabled it to operate at single supply voltage of 0.5 V [12].

3.10. Dynamic Power Management

In applications such as wireless sensor nodes the devices are shut down when not needed and they wake up when required, thus saving energy in sleep mode. One more method of saving energy is by using the techniques of Dynamic Voltage Scaling and Dynamic Frequency Scaling, which reduce the energy by Quadratic and Linear scale respectively

4. DISCUSSIONS

The SAR designs are gaining popularity for low power applications.

Paper	CMOS Technology Used (µm)	Supply Voltage (V)	Resolution (bits)	Sampling Rate (kS/s)	SNDR (dB)	SFDR (dB)	Area (mm^2)	ENOB (bits)	Power Consumption (µW)	FOM (pJ/conv step)
[1]	1.2	1	8	50	47.6	62.87	0.324	7.9	340	-
[2]	0.13	1.2	10	50000	54.4	61.8	0.05	9.18	0.826	29
[3]	0.13	1/0.4	10	1	56.7	67.6	0.19	9.1	0.053	94.5
		1/1							0.072	129.4
		0.3		10					0.118	11.8

[4]	0.13	0.4	8	60	49.7	58.8	0.171	7.97	0.538	8.97
		0.5		150					2.62	17.5
[5]	0.18	-	12	50	-	-	0.24	-	60	0.3
[6]	0.35	1.4	8	2	48.2	-	0.16	7.8	0.101	227
	0.18	1.1		2	46.3	-	0.06		0.027	79.9
[7]	0.18	1	8	250	44.28	-	0.08	7.06	2.86	85.7
[9]	0.18	1	8	200	49.8	63.2	0.63	7.96	19	165
			12	100	65.3	71		10.55	25	
[10]	0.065	1.2	10	100000	59	-	0.07	9.3	4500	0.062
[11]	0.25	1	8	100	47.8	60	0.053	7- 7.9	3.1	31
[12]	0.04	0.5	8	1100	46.8	58.2	0.0112	7.5	1.2	6.3

Table 1 Performance Comparison of some Low Power SAR ADCs

Some of the recently proposed low power SAR ADCs for different applications have been studied and surveyed and the analysis of these ADCs is done with respect to their performance parameters such as resolution, sampling frequency, SNDR, SNFR, power consumption, effective number of bits (ENOB), active area along with the figure of merit (FOM) and can be summarized by Table 1. The performance of these ADCs indicates that for a resolution of 8-12 bits, SAR topology is feasible enough to achieve low power operation while maintaining the other desired performance parameters. As the resolution is increased beyond 12 bits the power consumption of SAR increases drastically and hence requires new design techniques to reduce the power at higher resolution.

5. CONCLUSION

This paper presents a comprehensive study on the various design techniques proposed to achieve low power in SAR ADCs. It is observed that there is a trade-off between various performance parameters ADC like resolution, sampling speed, area, while designing an SAR for low power operation. Although the performance parameters vary with application, the SAR ADCs usually provide low power consumption for medium resolution (8-12 bits). As resolution is increased on the higher side, performance degradation occurs.

REFERENCES

[1] Mortezapour S, Lee E. A 1-V, 8-Bit Successive Approximation ADC in Standard CMOS Process. IEEE JSSC. 2000; 35(4): 642-6p.
[2] Liu C, Huang G. A 10-bit 50-MS/s SAR ADC With a Monotonic Capacitor Switching Procedure. IEEE JSSC. 2010; 45(4): 731-40p.
[3] Zhang D, Bhide A, Alvandpour A. A 53-nW 9.1-ENOB 1-kS/s SAR ADC in 0.13µm CMOS for Medical Implant Devices. IEEE JSSC. 2012: 47(7): 1585-93p.
[4] Abdelhalim K, MacEachern L, Mahmoud S. A Nanowatt ADC for Ultra Low Power Applications. Proceedings of the International Symposium on Circuits and Systems; 2006 May 21-24; Island of Kos. IEEE; 1507-10p.
[5] Fang X, Srinivasan V, Wills J, et al. CMOS 12 bits 50kS/s Micropower SAR and Dual-Slope Hybrid ADC. Proceedings of the IEEE 52nd International Midwest Symposium on Circuits and Systems; 2009 Aug 2-5; Cancun. IEEE; 180-3p.
[6] Hu W, Liu Y, Nguyen T, et al. An 8-Bit Single-Ended Ultra-Low-Power SAR ADC with a Novel DAC Switching Method and a Counter-Based Digital Control Circuitry. TCSI. 2013; 60(7): 1726-39p.
[7] Chin S, Hsieh C, Chiu C, et al. A New Rail-to-Rail Comparator with Adaptive Power Control for Low Power SAR ADCs in Biomedical Application. Proceedings of the International Symposium on Circuits and Systems; 2010 May 30-June 2; Paris. IEEE; 1575-78p.
[8] Długosz R, Iniewski K. Flexible Architecture of Ultra-Low-Power Current-Mode Interleaved Successive Approximation Analog-to-Digital Converter for Wireless Sensor Networks. VLSI Design. 2007; 2007:1-13p.
[9] Verma N, Chandrakasan A. An Ultra Low Energy 12-bit Rate-Resolution Scalable SAR ADC for Wireless Sensor Nodes. IEEE JSSC. 2007; 42(6): 1196-205p.
[10] Boulemnakher M, Andre E, Roux J, et al. A 1.2V 4.5mW 10b 100MS/s Pipeline ADC in a 65nm CMOS. Proceedings of the IEEE International Solid-State Circuits Conference; 2008 Feb 3-7; San Francisco. IEEE; 250-1p.
[11] Scott M, Boser B, Pister K. An Ultralow-Energy ADC for Smart Dust. IEEE JSSC. 2003; 38(7): 1123-9p.
[12] Shikata A, Sekimoto R, Kuroda T, et al. A 0.5 V 1.1 MS/sec 6.3 fJ/Conversion-Step SAR-ADC with Tri-Level Comparator in 40 nm CMOS. IEEE JSSC. 2012; 47(4): 1022-30p.
[13] Liu Y, Yuan C, Hung Y. A Capacitor Constructed Bypass Window Switching Scheme for Energy-Efficient SAR ADC. Proceedings of the International Symposium on Circuits and Systems; 2014 June 1-5; Melbourne VIC. IEEE; 1352-5p.
[14] Kropfitsch M, Riess P, Knoblinger G, et al. Dielectric Absorption of Low - K Materials: Extraction, Modelling and Influence on SAR ADCs. Proceedings of the International Symposium on Circuits and Systems; 2006 May 21-24; Island of Kos. IEEE; 545-8p.
[15] Sarpeshkar R. Universal Principles for Ultra Low Power and Energy Efficient Design. TCSI. 2012; 59(4): 193-8p.
[16] Razavi, Behzad. Principles of Data Conversion System Design. New York, Chichester, Weinheim, Brisbane, Singapore, Toronto: A John Wiley & Sons Publication; 1995.

Authors

Saima Bashir received her M.Tech degree in electronics and communication engineering from Shri mata Vaishno Devi University, Katra, India in 2016. She is currently pursuing her Ph.D. degree in electronics and communication engineering from National Institute of Technology Srinagar. Her research interests include data converters design, VLSI, analog and mixed signal VLSI design.

Suhaib Ahmed was born in Jammu, India, in 1991. He received the B.E. degree in electronics and communication engineering from University of Jammu, India, in 2012 and M.Tech. degree in electronics and communication engineering from Shri Mata Vaishno Devi University, India, in 2014. He is currently pursuing his Ph.D. degree in electronics and communication engineering from Shri Mata Vaishno Devi University, India. His research interests include data converters, quantum cellular automata, nanotechnology, application of wireless sensor networks in health and environment monitoring, biomedical signal processing and energy harvesting for biomedical implants. He is currently working on design and modeling of ultra low power mixed signal circuits for submicron devices. Mr. Ahmed is a member of IEEE, International Association of Engineers and Associate Member of Universal Association of Computer and Electronics Engineers.

Vipan Kakkar was born in Amritsar, India, in 1973. He received the B.E. degree in electronics and communication engineering from Nagpur University, India, in 1994 and M.S. degree from Bradford University, UK, in 1997. He received his Ph.D. degree in electronics and communication engineering from Delft University of Technology, Netherlands in 2002. He worked in Research & Development at Phillips, Netherlands as engineer and system architect from 2001 to 2009. Since 2009, he has been an Associate Professor with the Department of Electronics and Communication Engineering, Shri Mata Vaishno Devi University, Katra, India. His research interests include nanotechnology, ultra low power analog and mixed signal design, MEMS design, synthesis and optimization of digital circuits, biomedical system and implants design, audio and video processing. Dr. Kakkar is a Senior Member, IEEE and Life Member, IETE and has served as an Executive Member of IEEE, India and has published many research papers in peer reviewed journals and International Conferences. He has also authored a book on System on Chip Design and has served as an editorial board member of microelectronics and solid state electronics journal